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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/532,259	11/28/2005	Jean-Paul Dagois	PF020145	8623
24498	7590	02/05/2008		
Joseph J. Laks THOMSON LICENSING LLC 2 Independence Way, Patent Operations PO BOX 5312 PRINCETON, NJ 08543			EXAMINER MA, CALVIN	
			ART UNIT	PAPER NUMBER
			2629	
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			02/05/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/532,259

Applicant(s)

DAGOIS, JEAN-PAUL

Examiner

Calvin C. Ma

Art Unit

2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 May 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 May 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- ☒ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 05/26/2005.

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The references listed on the Information Disclosure Statement filed on April 25, 2005 have been considered by examiner; see attached PTO-1449.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamashita et al. (US Patent: 6,222,323).

As to claim 1, Yamashita discloses a device for displaying images comprising: an image display panel (1) comprising a first array (2) and a second array of electrodes (5)

(see Fig. 2, Col. 4, Lines 39-54) which serve an array of cells (6), where each cell is powered between an electrode of the first array and an electrode of the second array effecting between them an intrinsic capacitor C_i (i.e. the parasitic capacitance) (see Fig. 5, Col. 5, Lines 15-25) power supply means (V_{cc}) for generating a potential difference between two terminals (i.e. the two terminals are the V_{cc} terminal and the ground terminal), drive means (7, 9) adapted for successively connecting each electrode of the second array to one of the terminals of the power supply means, and, during a sequence of connection of an electrode of the second array, for simultaneously connecting one or more or even all the electrodes of the first array to the other terminal of the power supply means (i.e. all of the arrays are connected to the common power source and the common ground), wherein the drive means are adapted for being able, during each sequence of connection of an electrode of the second array, to transfer to the cell powered between each electrode of the first array and this electrode of the second array (i.e. the charge are move from the first electrode to the rest of the array) (see Fig. 5, 6, Col. 5, 39-58), the charge of the intrinsic capacitors of the other cells linked to the same electrode of the first array (i.e. the charge of the intrinsic capacitance are link to the electrode of the first array) (see Fig. 5, 6, Col. 5, 39-58).

As to claim 2, Yamashita teaches the device as claimed in claim 1, wherein the drive means are adapted so that, during each sequence of connection of an electrode of the second array, the transfer of charge via each of the electrodes of the first array is

avored at the expense of the connection of these electrodes to said power supply means (i.e. the charge are move from the first array electrode to the rest of the array and the electrode are set to ground or neutral) (see Fig. 5, 6, Col. 5, 39-58).

As to claim 3, Yamashita teaches the device as claimed in claim 1, wherein each image to be displayed being divided into pixels or subpixels to which are allocated luminous intensity data(i.e. the brightness level is set according to calculated data) (see Fig. 8, Col. 7, Lines 8-47), each cell of the panel being assigned to a pixel or subpixel of the images to be displayed, it comprises means (10) of processing said data so as to be able, during each sequence of connection of an electrode of the second array, to modulate the duration of connection t'_{a1} of each electrode of the first array to said power supply means and to modulate the duration of transfer of charge t'_{a2} of the intrinsic capacitors of the other cells linked to the same electrode of the first array, as a function of the luminous intensity datum of the cell powered between this electrode of the first array and this electrode of the second array (i.e. the brightness setter 10 according to external data set brightness level, which the controller 9 than apply to both the anode controller 7 and cathode controller 8 which allow the array of electrode to adjust the brightness by varying the intrinsic capacitance) (see Fig. 8, Col. 7, Lines 8-47).

As to claim 4, Yamashita teaches the device as claimed in claim 3, wherein the drive means (7,8) are adapted so that, during each sequence of connection of an

electrode of the second array, said connection of each electrode of the first array to said power supply means is carried out, as appropriate, at the end of a sequence and said transfer of charges is carried out, as appropriate, at the start of a sequence (i.e. since the sequence is the scanning of the data to each of the cell the electrodes must adjust at the beginning of a given line which is also the end of the previous scanning line, therefore both connection to power and transfer of charges happens at these junctions) (see Fig. 1, Col. 5, Lines 18-58).

As to claim 5 and 6, the adapted to clauses used in claim 5 and 6, are analyzed to have not limited the scope of the claims and are therefore rejected on the same ground as claim 1 which they are depended on (see MPEP 2111.04).

As to claim 7, teaches the device as claimed in claim 1, wherein said cells are electroluminescent (see Fig. 1, Col. 5, Lines 10-15).

As to claim 8, teaches the device as claimed in claim 7, wherein each cell comprises an organic electroluminescent layer (see Fig. 1, Col. 5, Lines 10-15).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negated by the manner in which the invention was made.

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita in view of Aziz et al. (U.S. Patent 6,811,896).

As to claim 9, Yamashita teaches the device as claimed in claim 8, but does not explicitly teach wherein the thickness of said layer is less than or equal to 0.2 μm . Aziz teaches the layer of organic electroluminescent layer being equal to 200 nanometers (which is exactly 0.2 μm) (see Col. 1, Lines 55-63).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the thickness layer of Aziz in the overall display design of Yamashita in order to, "reduce OLED shorting." (Aziz Col. 2, Lines 40-46).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ouellete et al. (US Patent: 7,027,013), Bock et al. (US Patent: 6,417,868), Feldman (US Patent: 6,121,961), Iketsu et al. (US Patent: 6,369,516) and Ushigusa et al. (US Patent: 6,229,267) are cited to teach similar OLED designs.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Calvin Ma whose telephone number is (571)270-1713. The examiner can normally be reached on Monday - Friday 7:30 - 5:00 EST.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571)272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Application/Control Number:
10/532,259
Art Unit: 2629

Page 8

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Calvin Ma
February 1, 2008


CHANH D. NGUYEN
SUPERVISORY PATENT EXAMINER